# Ripple Adder

## Block Diagram

Diagram

Description automatically generated

## Propagation Time Estimation

## Time Taken to add 4 pairs of numbers

## Verilog Code

---*code snap---*

## Simulation Result

A picture containing graphical user interface

Description automatically generated

Add 4 numbers with 5ns time gap. Since this is a simulation, we cannot see the propagation delay of ripple adder.